

IE1204_5. Digital Design.

Presentations from the year 2013-2014

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Contents

Introducing digital technology. Binary numbers.

 [F1intro_eng.pdf](#)

Digital Design - everywhere

- 40-100 microprocessors in a car, the development of electronics

- Why is digital technology so successful?

- Simplicity, immunity of electromagnetic disturbances.

- Analog/digital, sampling

- Immunity. Capturing data is still critical.

More soon in the course ...

- Boolean algebra, axioms, rules and laws.

- Serial and parallel connected switches is the technical background.

- Nowdays gates. Just one sort of gate is enough! CMOS NAND ...

- Memoryfunction - CMOS NAND.

- See-of-Gates

- How does one design with a billion gates?

- CAD-tools, Hardware description languages. The designprocess.

Binary numbers.

- Decimal number system. Binary system. Octal number system. Hexadecimal number system.

- Conversion between decimal and binary numbers.

Logic functions, gates and circuits. Boolean algebra.

 [F2grindar_eng.pdf](#)

- Switch, implementation of logic functions.

- AND, OR NOT.

- Truth table.

- Logic gates. AND, OR, NOT

- Network function? Timing Diagram, Truth Table.

- Multiple logic circuits can implement the same function.

Axioms of Boolean Algebra.

- The Venn Diagram.

- Boolean algebra theorems. Duality.

- Two- and Three-Variable Properties.

- Ex. 17 a) The Consensus Property.

Different notations.
Analysis and Synthesis.
The Truth Table (a guess?).
Logic Function - implementation with gates.
Minimize with the Boolean algebra - much simpler implementation.
Minterm and Maxterm.
SOP- and POS- form. Duality.
NAND - NOR
Complete logic - just one type of gate is needed.
De Morgan's theorem - bubblegates.
Inverters with NAND. AND, OR - logical functions with just NAND.
Universal sets of gates.
XOR and XNOR.
Example - three-way light control.

**Bin-Hex-Okt. Boolean Algebra, Theorems. Venndiagram. Logic Gates.
Minterm, Maxterm. SOP- POS- form, Complete logic . Truth Table and
Timing Diagram.**

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Dec - Bin - Hex - Okt.
Ex. 1.1c Dec to Bin.
Ex. 1.2a Bin till Dec.
Ex. 1.3c Bin/Okt/Hex
Ex. 3.2 De Morgans Theorem illustrated with Venn Diagram.
Ex. 5.1 minterm
Ex. 3.3a Truth Table - minterms - simplified expression
Ex. 4.1 a, b, c, h Boolean algebra.
Ex. 4.4 De Morgans Theorem.
Ex. 4.5 a different gates.
Ex. 4.7 Timing Diagram and Truth Table.
Ex. 4.12 From text to Boolean equations.
Ex. 5.2, Ex. 5.3 SOP and POS canonical form.
Ex. 5.5 NAND-gate.
Ex. 4.11 symbols used for gates.

CMOS. Integrated circuits (7400-series).

 [F3cmos_eng.pdf](#)

A transistor is a switch with no moving parts.
P and N type. The structure of CMOS circuits.
CMOS inverters. voltage levels (unstable point).
CMOS - dynamic power dissipation.
NAND-gate, NOR-gate.
Three-state.
Pass-gate.
MUX - implementation - Pass-gate.
XOR - implementation - Pass-gate.
Gate delays. Capacitive load.

Optimized structures.
FAN-out (buffer) and FAN-in (tree structure).
Critical path.
Lookup-table, eg. XOR.
74-series standard circuits.
CMOS - low current consumption?

Combinational networks. Karnaugh diagrams. Twolevel minimization. Multi-level minimization.

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Function (OR) with minterms. Minimization with algebra.
Function (OR) with maxterm.
Function (OR) Minimization with Venn Diagram.
Graphic minimization method.

Boolean numberspace, n-dimensional-cubes. Hypercubes.

Ex. 3.4 representation of logic function with cube. Cubical Technique for Minimization.
Gray-code.
3D-cube - 2D-diagram.

Karnaugh-map

"Neighbors" (adjacent minterms), merging of 1's.
Merging of 0's.
Minimization Example. Prime- Essential- Redundant- implicants.

Twolevel minimization. Sub-cubes. XOR/XNOR.

Karnaughmap with 5 or 6 variables.
The use of Don't care.

Multi-level minimization.

Factoring.
Functional Decomposition.

Digital arithmetic: Number representation of integers.

Different adder circuits.

Addition and Subtraction. Comparator. Design trade-offs.

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Integers, sign-magnitude, one-complement, two-complement.
Fast conversion, sign extension.
Example of addition. $5+2$, $5-2$. Overflow $5+5$, $-5-5$.
Subtraction = addition with twocomplemented number.
How to detect overflow with two carry-bits.
Halfadder. Fulladder.
Odd parity function.
Fulladder with two Halfadders.
Example - three-way light control - revisited (XOR-parityfunction).
Paritetycheck.
Ripple-Carry-adder. Carry-function with NAND-gates.
XOR with NAND-gates.
Faster adder. Generate and Propagate functions.

Carry look ahead adder.
Hierarchical expansion.
Carry select adder.
ADD/SUB-unit. ALU. Comparator.

Digital arithmetic: Multiplication and Division.

Number representation: fixed-point and floating-point.

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Multiplication of two positive integers.
Multiplication with the sign bit.
Multiply only positive numbers, adjust result sign if needed.
Hardware for multiplication of two positive numbers.
Carry Save multiplication circuit.
Multiplication and division by powers of two.
Barrelshifter.
Division between positive integers. Quotient and remainder.
Division circuit - hardware.
Division by negative integers. Use positive numbers and adjust the result sign if needed.
The difference between logical and arithmetic shifts.
Fixpoint-numbers. Q-format.
Float. IEEE-754.
Addition with floating point, Multiplication / Division with float.
Hardware for floating point operations, floating point unit.

Karnaughmap. Minimization with K-map. Don't Care. Level indicator for water tank.

CMOS-gates. Threestate-gate. PULL-up and PULL-down network.

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Ex. 6.1, 6.2 Karnaughmap.
Ex. 6.4 from NOR to NAND.
Ex. 6.5 Minimize with K-map.
Ex. 6.8 Don't care.
Ex. 8.2 Level indicator for water tank.
Ex. 7.3 CMOS-gate.
Ex. 7.4 Three-state gate.
Ex. 7.5 Pull-up network and Pull-down network.

Multiplexer and demultiplexer, encoder and decoder.

Shannon decomposition. Introduktion to VHDL.

 [F7kombinatorikkretsar_eng.pdf](#)

PLD-circuits - fan-in is limiting. Solution MUX-tree.
Logic functions with MUX. NOT AND OR XOR.
Hierarchies of MUX.
Shannon decomposition.
MUX - Look-up table.

Decoder, Demultiplexor, ROM, Encoder, Encoder, Transcoder.
VHDL introduction.
Entity, Architecture. Description Styles: Structural, Sequential, Dataflow.
Port, datatypes, signals.
Generate. Testbench.

Transcoder. Shared gates in PLA-circuit. Float.
2-complement Negative numbers. Register as a ring of integers. Fulladder, Subtractor circuit.
Multiplication and division. Float. Comparator flags. Carry-save multiplier.

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Ex. 8.4 Transcoder 7-4-2-1 kod. Shared gates in PLA-circuit.
Real numbers.
Ex. 1.2b conversion from real binary to decimal.
Two-complement, registers. Different registers lengths.
Ex. 1.8 two-complement notation.
Ex. 2.2 Subtract with the two-complement method.
Ex. 2.3, 2.4 Multiplication and division.
Float.
Ex. 2.5 Storage of float.
BV Ex. 5.10 Comparator circuit.
BV Ex. 5.12 Multiplication circuit - Carry-save.

Shannon decomposition. Fulladder and Parity-function with FPGA-cell LUT+MUX.
Barrel shifter. ACTEL FPGA-block. VHDL logic functions.

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Ex. 8.6 4-1 MUX function generator for OR.
BV 6.1 realize a function with a decoder.
Ex. 8.7 Majority function: gate circuit, 8-1 MUX, 2-1 MUX + gates, only 2-1 MUX.
BV. 6.5 function with 2-1 MUX + gates.
Ex. 8.8, 8.9 FPGA-cell as Fulladder and as Parity function.
BV. 6.31 Shifter with MUX.
BV. 6.32 Barrel shifter.
BV. 6.16 Function with Actel ACT1 logic module.
BV. 2.51a VHDL functions.
BV. 6.21 VHDL encoder.
Designing with MUX and few gates.

Memory elements: Latches and flip-flops. Counter.

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MUX that latches its value. D-latch.
The input values that get gates locked. SR-latch with NOR gates.
Latch with NAND-gates.
D-latch with modified SR-latch.

- Setup & Hold-time
- Register - inverted outputs always available.
- Every other pulse - not possible with a Latch.
- Clocked flip-flops - Master-Slave flip-flop.
- Edgetriggered D-flip-flop.
- The difference between latches and clocked flip-flops.
- Every other pulse - with D-flip-flop.
- Clear and Preset. Synchronous / Asynchronous reset.
- JK and T-flip-flop. Design with D-flip-flop.
- Timing Analysis - what is the maximum clock frequency.
- Shiftregister.
- Counter. Asynchronous Ripplecounter, Synchronous counters.
- VHDL for flip-flops and latches.
- Process. Latch, D-flip-flop, synchronous reset, asynchronous reset. Counter.

Synchronous sequential circuits: State Machines. Moore and Mealy machine.

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Moore machine.

- State Memory (register) with D-flip-flops.

Design Example "two successive".

- State Diagram. State Table.

- State assignement. State-assigned table.

- Transition logic. From state-assigned-table to K-map.

- Output logic. The implementation.

- Timing diagram.

- With the notation of the exercise booklet.

Mealy machine.

- State Diagram - Mealy, State Table, State-assigned table.

- Implementation. Timing diagram.

- Mealy with output-register. Timing diagram with register.

State assignement considerations.

- Binary code, Gray code, OneHot code.

Latches and flip-flops. SR-latch. D-flip-flop. T-flip-flop. JK flip-flop. Flip-flop timing parameters. Asynchronous/Synchronous binary counters. Up/Down counter. Multifunction-shift registers.

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- Ex. 9.1 SR-latch, timing diagram.

- Ex. 9.4 toggle with a D-flip-flop

- Ex. 9.3 Timing diagram with a D-flip-flop.

- Ex. 9.5 The "Universal" JK-flip-flop as D and as T.

- Ex. 9.6 D-flip-flop timing parameters.

- BV. 7.5 Asynchronous Counter

- BV. 7.16 Up/Down with T-flipflops

- BV. 7.17 Up/Down with D-flipflops

- BV. 7.13 Multifunction Shift-register.

- BV. 7.24 Maximum clockfrequency for counter.

State minimization, Analysis, ASM Charts, Formal FSM model

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Moore/Mealy input-output.

Leftover states.

Reset-generator chip.

Counter {0,1,2}, {3?}

Take care of the {3}-state. Final state diagram.

State minimization.

A simple method - not the optimal method that the CAD tools uses.

State minimization. "Not equivalent state."

Not equivalent if: different output, any successor state has different output.

Make Partitioning to groups that may be equivalent.

When no further partitioning is possible, we have the minimal number of states.

The value of state minimization.

Analysis of sequential circuits.

Think "Moore machine", analyse the combinational circuits.

Karnaugh maps - the next state decoder - encoded state table.

State Table - State Diagram.

ASM charts.

"two successive" as ASM-chart, Moore-type, Mealy-type.

Formal mathematical model for the state machine.

Bottle Vending machine. State Minimization - the kindergarten version.

 [flaskautomat_eng.pdf](#)

 [StateMini_eng.pdf](#)

Programmable logic. Design of sequential circuits in VHDL.

 [F11fpgaVHDL_eng.pdf](#)

PLD-structure. PLA-structure. PAL-structure.

PLD macrocell.

CPLD MAX, JTAG-port.

FPGA. Structure. LUT, logic block. Routing matrix.

ASIC, gate array. Full custom.

Sequential Circuits with VHDL.

Processes in VHDL. Next-state decoder, Output decoder, State register.

Internal signals. Current state, the next state.

Example. Bottle vending machine. VHDL-code.

State machines. Moore machine, Mealy machine.

Analysis. Description. Various state assignment, binary, gray, oneHot.

Asynchronous reset. State Diagram - asm chart.

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Ex. 10.1, Ex. 10.2 analysis of a circuit.
(Ex. 10.4 stop state, loss state, isolated state)
Ex. 10.5 behavior based on the state diagram.
Ex. 10.6 Moore-machine "three successive".
Ex. 10.7 different olika state assignment. Reset.
Ex. 10.8 Counter. State the next state decoder equations.
BV. 8.36 ASM chart.
Ex. 10.10 State minimization.

Asynchronous sequential circuits: analysis, synthesis, state minimization, state encoding.

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Only one input is changed at a time - the golden rule.
SR-latch with NOR gates. Delay block in place of the D flip-flop.
Next state expression. State Table = Flow Table. Stable states.
State-assigned table = Excitation Table.
Flow Table and Excitation Table, Moore.
Flow Table and Excitation Table, Mealy.
Asynchronous sequential Moor-compatible, Mealy compatible.
Analysis. D-latch, Master-Slave D-flip-flop.
Flow Table - impossible state transitiond (golden rule). D-flip-flop State Diagram.
Synthesis.
Example "toggle circuit".
Create the State Diagram. Flow Table.
What is a good state assignment? Hammingdistance "1".
example good and bad State assignment.
Problem with instable states.
Solution. Transfer state.
Extra states - moore dimensions, hypercubes.
Karnaughmaps - Hazard-cover (moore later).
Resulting circuit.
State minimization, asynchronous sequential circuits.
Partitioning procedure - state reduction.
Compatibility Groups (either Moore or Mealy).
Merger diagram.
BV. 9.8 Illustrative example.

Asynchronous state machines, racing, the complete primimplicator-form. Analysis SR latch. Synthesis of DETFF-flip-flop. Analysis - flip-flop.

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- Ex. 11.1 Glitches - hazard cover.
- Ex. 11.2 Analysis SR-latch.
- Ex. 11.3 Ringoscillator.
- Ex. 11.4 circuit - dubbeedge triggered flip-flop
- Ex. 11.5 Synthesis of DETFF-flip-flop.
 - Possible in+out combinations. DETFF Truth Table.
 - Flow Table.
 - State reduction. The reduced Flow Table.
 - State code assignement. Exitationtable.
 - Karnaughmaps. Next state equations.
- Ex. 11.6 Analyse circuit. Wich type of flip-flop is it?

Asynchronous sequential circuits: hazard, metastability, asynchronous input signals. A design task.

 [F13asyFSM2_eng.pdf](#)

Hazard.

- Different types of hazard. Static hazard. Dynamic hazard.
- Significance of Hazards? Metastability. Setup and Hold time (= metastability-protection) Synchronization of input signals.

Construction of a set-dominant SR-latch.

Semiconductor memories. What's inside a Microcomputer?

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- ROM-implementation of combinatorial functions.
- ROM-implementation (+register) of the sequential circuit.
- RAM, SRAM, DRAM.
- FLASH, EEPROM, EPROM.
- The Microprocessor.
 - Register.
 - Program-counter.
 - Bidirectional register, databus, two-port-register.
 - Register file.
 - Possible instructionformat.

Address Decoding of ROM, SRAM, and I/O.

Combinatorial network with 5 variables. Binary squarer. Step motor controller. Algorithmic State Machine ASM.



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Ex. 12.1 Dynamic memory.

Ex. 12.2 Address Decoding of ROM and SRAM.

Ex. 12.3 Address Decoding of I/O.

Exam Refresher.

Ex. 6.10 Combinatorial network with 5 variables.

Ex. 8.1 Binary squarer.

Ex. 10.9 Step motor controller.

Algorithmic State Machine ASM.

BV. 10.5 Dividerare med successiva subtraktioner.

algorithm (pseudocode) - ASM-diagram.

Datapath - detailed ASM chart.

Designing the control logic.